Amendments to Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. - 15. (canceled)

16. (currently amended) A semiconductor topography comprising an upper layer formed conformally upon a non-planar lower layer, wherein the upper layer is present across the entire topography, and an average thickness of the upper layer in a region adjacent to an outer edge of the semiconductor topography is approximately 5% to approximately 30% less than an average thickness of the upper layer in a region comprising a center of the topography.

17. (original) The semiconductor topography of claim 16, wherein the region having a lower average thickness extends greater than approximately 3 mm laterally from the outer edge of the semiconductor topography.

18. - 23. (canceled)

24. (new) The semiconductor topography of claim 16, wherein the lower layer comprises a plurality of spaced structures.

25. (new) The semiconductor topography of claim 24, wherein the plurality of spaced structures comprise a polish stop material.

26. (new) The semiconductor topography of claim 24, wherein one of the spaced structures is arranged within 4 mm from the outer edge.

27. (new) The semiconductor topography of claim 24, wherein the plurality of spaced structures are selected from the group consisting of gate structures, contact structures, local interconnect structures, conductive plugs, shallow trench isolation structures, dielectric layers, and conductive layers.